IN THE CLAIMS

Claim 1 (currently amended): A hard disk storage system, comprising:

a magnetic disk;

a head for writing data to the disk;

a preamplifier for orienting a current through the head in a desired direction responsive to a data signal, comprising:

a first pair of transistors of a first type driven by the data signal coupled to across said head;

a second pair of transistors of a second type coupled across said head and driven by a transistor of the first type, such said first and second pairs of transistors provide a current path through the head in a direction responsive to the data signal;

where the first transistor type is slower than the second transistor type, so that one terminal of the head is pulled to a first voltage level through one of the first pair of transistors and another terminal of the head is pulled to a second voltage level through one of the second ~~transistor~~ pair of transistors at substantially the same time.

Claim 2 (original): The hard disk storage system of claim 1 wherein the first transistor type is a PNP transistor type.

Claim 3 (original): The hard disk storage system of claim 2 wherein the second transistor type is an NPN transistor type.

Claim 4 (original): The hard disk storage system of claim 1 wherein the first transistor type is an NPN transistor type.

Claim 5 (original): The hard disk storage system of claim 4 wherein the second transistor type is a PNP transistor type.

Claim 6 (currently amended): The hard disk storage system of claim 1 wherein the preamplifier further comprises a trans-resistance circuit between for switching one of the second ~~transistor~~ pair of transistors.

Claim 7 (currently amended): The hard disk storage system of claim 6 wherein the trans-resistance circuit comprises:

a third pair of transistors for controlling respective ones of the second pair of transistors; and

circuitry for rapidly charging one of ~~the~~ including a third pair of transistors and discharging the other of said third pair of resistors responsive to the data signal, such that one of the second pair of transistors is turned on and the other of the second pair of transistors is turned off responsive to the data signal.

Claim 8 (original): The hard disk storage system of claim 1 wherein the data signal is a differential data signal.

Claim 9 (currently amended): A preamplifier for controlling the direction of current through a head of a hard disk drive assembly, comprising:

a first pair of transistors of a first type driven by the data signal coupled to across said head;

a second pair of transistors of a second type coupled across said head and driven by a transistor of the first type, such said first and second pairs of transistors provide a current path through the head in a direction responsive to the data signal;

where the first transistor type is slower than the second transistor type, so that one terminal of the head is pulled to a first voltage level through one of the first pair of transistors and another terminal of the head is pulled to a second voltage level through one of the second pair of transistors ~~transistor~~ at substantially the same time.

Claim 10 (original): The preamplifier of claim 9 wherein the first transistor type is a PNP transistor type.

Claim 11 (original): The preamplifier of claim 10 wherein the second transistor type is an NPN transistor type.

Claim 12 (original): The preamplifier of claim 9 wherein the first transistor type is an NPN transistor type.

Claim 13 (original): The preamplifier of claim 12 wherein the second transistor type is a PNP transistor type.

Claim 14 (currently amended): The preamplifier of claim 9 wherein the preamplifier further comprises a trans-resistance circuit between for switching one of the second ~~transistor~~ pair of transistors.

Claim 15 (currently amended): The preamplifier of claim 14 wherein the trans-resistance circuit comprises:

a third pair of transistors for controlling respective ones of the second pair of transistors; and

circuitry for and including rapidly charging one of ~~the~~ a third pair of transistors and discharging the other of said third pair of resistors responsive to the data signal, such that one of the second pair of transistors is turned on and the other of the second pair of transistors is turned off responsive to the data signal.

Claim 16 (original): The preamplifier of claim 9 wherein the data signal is a differential data signal.

Claim 17 (withdrawn): A trans-resistance circuit for rapidly enabling one of a pair of transistors of a write driver and disabling the other of the pair of transistors of the write driver responsive to a data signal, comprising:

circuitry for charging a first node responsive to a first state of the data signal and actively discharging the first node responsive to a second data signal; and

circuitry for charging a second node responsive to the second state of the data signal and actively discharging the second node responsive to the first data signal.

Claim 18 (withdrawn): The trans-resistance circuit of claim 17 wherein said circuitry for charging the first node comprises:

a first current source;

a second current source coupled to the first node;

a third current source;

a fourth current source coupled between the second node, where each current

source supplies the same amount of current;

a first transistor for selectively providing a path between the first current source and the first node, responsive to the data signal;

a first resistor coupled between the third current source and the first node; and

a second transistor for selectively providing a path between the second node, responsive to the data signal, such that the data signal enables one of the first and second transistors and disables the other of said first and second transistors;

a second resistor coupled between the third current source and the second node, such that current is drawn through said first resistor when said first transistor is disabled and the second transistor is enabled, thereby charging the first node, and current is drawn through the second resistor when said first transistor is enabled and the second transistor is disabled , thereby charging the second node.

Claim 19 (withdrawn): The trans-resistance circuit of claim 18 wherein said first node drives a third transistor and the second node drives a fourth resistor.

Claim 20 (withdrawn): The trans-resistance block of claim 19 wherein the third transistor drives said one of the pair of transistors of the write driver and the fourth transistor drives the other of the pair of transistors of the write driver.